

INTRODUCTION

First introduced in 2004, the LXI instrumentation platform has quickly gained acceptance in the functional test and data acquisition industries as a viable communications bus alternative to GPIB for rack and stack instruments. To support the market demand, most LXI products to date have been released at the minimum requirements level (Class C). Since LXI is based on Ethernet, it is also well-suited for applications where the instrumentation hardware is distributed throughout a test system, lab or large test article and can be separated by a significant distance from the host controller. Fortunately, the LXI Class A definition allows distributed instruments to achieve high levels of synchronous and asynchronous behavior, typically found in chassis-based systems that utilize a backplane, without compromising analog performance.

BACKPLANE BENEFITS

To understand the merit of LXI Class A instrument designs for demanding test and data acquisition applications, it is helpful to review the benefits of successful backplane-based platforms such as VXI and PXI. The common thread in a backplane-based platform is resource sharing, which can lead to a reduction in overall system footprint and hardware costs while increasing system performance. These resources include:

- **Communications Bus:** Successful open architecture platforms depend on well-defined industry standards for controlling devices and transferring data with very high bandwidth. VXI (VMEbus) and PXI (PCibus) employ high-speed communications busses that are shared by all instruments plugged into the mainframe.
- **System Clock:** Discrete instruments that plug into a backplane share the same system oscillator, effectively making the devices immune to delay and jitter drift differences that occur when devices are distributed with free-running clocks. When using multiple mainframes in a distributed system, IRIG-B or GPS receiver modules are typically used to give each subsystem the same relative notion of time.
- **Trigger Lines:** VXI and PXI each employ eight-line hardware trigger busses that are most commonly used for device-to-device handshaking and synchronization. These trigger busses can streamline asynchronous processes and greatly increase test throughput, providing the highest degree of determinism for communication between instruments.
- **Power Supply and Cooling:** Mainframe-based systems have a single power supply design that is distributed across the backplane and shared by all modules. Architectures like VXI also have well-defined cooling specifications. Power supplies are often the most expensive component of a mainframe since they must deliver enough power to support complex instruments and are often used at less than 50% capacity. In contrast, LXI instruments have optimized power supplies and cooling systems, which result in more efficient and lower cost designs.
- **Analog Bus:** This backplane feature is seldom used in plug-in module designs. The VXI platform, for example, provides a 12-line analog bus that can be used to share signals between devices within the mainframe. This has the potential advantage of reducing external system cabling. However, the analog bus is generally used between instruments that are supplied by the same vendor. Many LXI designs that utilize plug-in modules now incorporate instrument-specific internal analog busses to simplify external wiring.

A VERSATILE COMMUNICATIONS BUS - LXI CLASS REVIEW

The LXI class specification relies on the LAN/Ethernet communications bus at its core. LAN is a well-established bus that is ubiquitous in today's corporate environment. It provides a simplified infrastructure, readily accessible cabling, and a very stable platform that has consistently evolved

over the last 30 years while maintaining backward compatibility. Gigabit Ethernet provides bandwidth that rivals the VXI and PXI platforms. LXI adds three layers of classes on top of LAN along with increasing capability at each level. Figure 1 illustrates the LXI class structure.

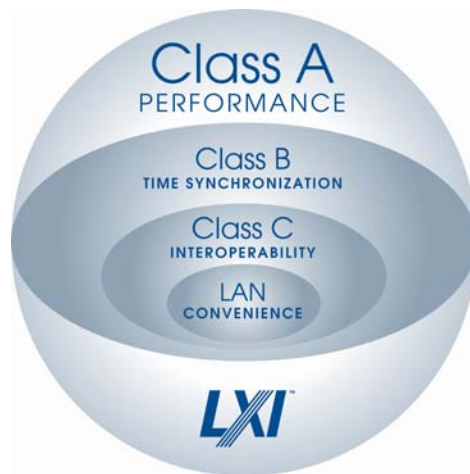


Figure 1: LXI Class Structure

Class C provides the critical requirements for ensuring interoperability within an open architecture platform where hardware from multiple vendors often resides on the same test network. Class B includes Class C definitions while enabling distributed devices to obtain a common absolute time reference through the IEEE-1588 protocol. Class A instrumentation includes Class C and Class B capabilities while providing a highly deterministic framework for handling asynchronous communication between devices with a high performance trigger bus. Class A, as a superset of the LXI classes, defines the framework for distributing backplane-like performance in data acquisition and ATE applications.

LXI SYSTEM CLOCK - UNIFYING A NOTION OF TIME

Simply speaking, a clock keeps time using an oscillator and a counter. For example, an ideal 10 MHz oscillator will produce exactly ten million clock edges to a counter in one second. Since all oscillators have errors, the counters on distributed boxes will vary and stray from a reference. In a backplane system, all devices see the same clock and thus the same error. So, in relative terms, the instruments in a backplane are very tightly synchronized. With discrete instruments, each device contains its own oscillator, resulting in a system that has varying clock inaccuracies as well as jitter. These differences between devices are not constant (e.g., due to ambient temperature variations) and cannot be easily factored out.

In distributed data acquisition and monitoring applications, a synchronized notion of time is necessary to correlate acquired data. Multiple devices that observe and record a single event, such as a destructive test, must have accurate notions of time with respect to a reference clock. Any errors will result in the misinterpretation of data that can translate to costly design errors or test reruns. With LXI Class A and B, use of the IEEE-1588 standard ensures that distributed devices have the same notion of wall clock time by establishing which device has the most accurate clock and assigning it as the master, while all other devices are designated as slaves. The master and slaves execute offset and delay compensations at regular intervals with the potential to synchronize devices to tens of nanoseconds or better. All measurements are returned with an IEEE-1588 timestamp, making it easy to correlate data from multiple instruments.

An accurate notion of time has benefits that extend beyond time-stamping and data correlation. Once all devices agree on a precise time, actions based on future times can be scheduled. Devices can be precisely synchronized to start an acquisition based on time (time-based events).

A sequence of events can also be scripted based on time intervals once the operation of a system has been characterized through event logging. Additionally, IEEE-1588 offers advantages over IRIG-B and GPS implementations. Since receiver modules are not required, the cost and complexity of the system is reduced.

LXI TRIGGER LINES - DISTRIBUTING FREQUENCY STANDARDS

A major benefit of backplane systems is the ease at which a frequency standard is shared by all modules. It is quite common to feed a high-stability oscillator (e.g., a rubidium standard) into the mainframe and distribute it to all the modules. This increases measurement accuracy and stability for instruments including counter/timers, arbitrary waveform generators, and other devices whose own accuracy is dependent on the system clock. In data acquisition applications where multiple channels must be simultaneously sampled and tightly synchronized, all devices in the backplane have the same time base and thus see the same jitter. Delay is restricted to propagation across the backplane (picoseconds).

Large-scale data acquisition applications present challenges that mainframe-based systems are not designed to handle. The size of the test article can make it difficult to place the mainframes close to the transducers. Traditionally, these systems had long cable runs connected to a centralized instrumentation room, resulting in increased susceptibility to noise and reduced data reliability. The majority of these signal integrity issues can be avoided by placing the test hardware closer to the transducers with shorter cables.

The benefits of distributing precision measurement devices across distances and closer to the test article were demonstrated in a large-scale structural test that took place during the certification of a wing design by a major aircraft manufacturer. Aircraft wings are required to withstand at least 150% of the maximum load that they would typically experience in service. Structural tests are used to validate how closely the analytical models of the designs have achieved this objective. Transducers are placed along the wing to help assess stress from loading mechanisms. During this test, Ethernet was used to help place the signal conditioning and data acquisition hardware as close to the transducers as possible to maintain integrity of the signals. Hundreds of discrete precision instrumentation boxes collected data from thousands of strain gages placed on the aircraft wing. The instrumentation boxes were connected to a single host controller over LAN.

To precisely align the data for post-test analysis, the oscillators on each box had to experience the same jitter and delays to guarantee accuracy. Thus, a master oscillator was shared by all the boxes. The LXI Class A trigger bus was the only mechanism able to distribute physical signals (direct transfer of a 50 MHz oscillator), as well as the sync/arm/trigger signals, and achieve the accuracy required by the application. In effect, all the boxes performed as if they were modules plugged into a single backplane even though they were separated by considerable distances.

FLEXIBLE TRIGGERING MODELS

DMMs and relays are often used together to multiplex many signals into a single measurement device. A popular method used in pacing the sequencing of switch and measure functions in GPIB-based systems depends on polling the operation complete bit (OPC). Another method involves the use of wait/delay statements to determine when the DMM has finished a measurement or when a switch has settled. This places a burden on the controlling processor that adds overhead to the total test execution time. Today's intelligent switching systems have on-board memory that can host a list of switch channels to be scanned and I/O that can receive and issue hardware triggers to assist in sequencing and greatly reduce test time.

The IviLxiSync trigger model offers a few different methods that allow the software to take advantage of the instrument's intelligence. Instead of polling OPC bits, an LXI Class A DMM can

be programmed to broadcast an LXI Event Message (e.g., LAN0) when it has completed a measurement. The LXI Class A switch listens for that broadcast message and closes the next channel in its pre-programmed list. Another LXI Event Message (e.g., LAN1) is sent by the switch indicating that it has settled and is ready for the DMM to initiate a measurement. Arbitrary message IDs are also supported to further enhance the test development and integration process. For example, LAN0 could be "MeasComplt" and LAN1 could be "RelaySettld." Because the switch and DMM pace the acquisition, the host controller is removed from the process, which provides a more efficient test. Of course, there is some degree of latency depending on LAN traffic as messages get passed back and forth across the Ethernet wire. However, the impact of latency as a percentage of overall test time is significantly less than when compared to polling or delay statements.

Since LXI Class A devices share a precise notion of time, switch/measure sequences can also be scripted based on references to time. In this paradigm, a DMM and switch use time-based triggers to pace the sequence of switch closures and DMM measurements. Instead of the DMM and switch issuing message-based triggers when they have settled, the trigger sources for each device become an absolute time based on IEEE-1588. It is usually simple to determine how much time it will take for a DMM to return a measurement, given a specific range and function, and how much time it takes for a relay to settle. The triggers to the devices are generated at regular intervals based on how much time has elapsed, thus improving test efficiency. This model can get considerably more complex, however, if the programmer must account for DMM range and function changes due to additional settling delays.

When test instruments are relatively close, such as in ATE systems, the LXI Class A trigger bus offers a familiar mechanism that is analogous to the VXI or PXI trigger bus. Therefore, the lviLxiSync programming model for hardware triggers is intuitive for developers familiar with those platforms. Since the DMM and switch are capable of sending and receiving the pacing triggers over hardware lines (e.g., LXI0 and LXI1), the result is a highly deterministic sequence with latency that matches those found in backplane-based systems. LXI Class A devices offer a powerful combination of LAN and hardware triggering mechanisms that allows users to optimize their test system performance, whether the architecture is distributed or in a traditional rack environment. Figure 2 illustrates two of the different implementations that LXI Class A offers to facilitate handshaking between devices.

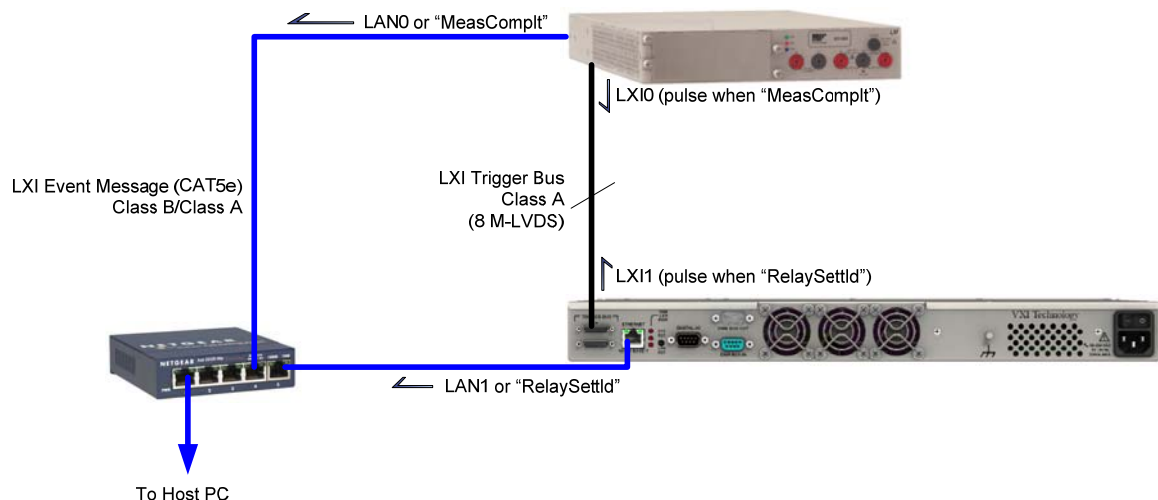


Figure 2. Inter-module handshaking methods using LXI Class A

An LXI Class A DMM (VTI EX1266), and LXI Class A switch (VTI EX1206 – rear view) are shown. The LXI trigger bus provides the same functionality as a backplane trigger bus, and is used to

transmit pulses between devices indicating operation-complete conditions with near-zero latency. An alternate approach utilizes the standard LAN cabling to send and receive LAN-based messages to communicate the same information. In both cases, the host controller is removed from the sequencing process.

A NATURAL FIT FOR HYBRID SYSTEMS

For many years, multi-platform systems have been recognized as practical implementations for test systems. It is not uncommon for a single test system to include VXI, PXI, or even LXI platforms. LXI Class A bridge devices provide the means for synchronizing LXI devices and those in mainframe-based systems together in a single test network. To accomplish this, a Class A bridge device plugs into the mainframe (e.g., VXI slot 0) to enable the mainframe to connect to a host PC over LAN and reside on an LXI test network communicating with native LXI devices.

For example, an LXI-VXI slot 0 bridge, such as VTI's EX2500A, provides a web-based utility that is analogous to other popular VISA graphical command utilities. The bridge is capable of converting VXI TTL triggers into LXI LAN-based messages over Ethernet, or into LXI compatible triggers over the LXI M-LVDS trigger bus. Conversely, the slot 0 bridge can accept LXI LAN-based messages and LXI hardware triggers and convert them into VXI TTL triggers as illustrated in Figure 3.



Figure 3: EX2500A LXI-VXI Class A Slot 0 Bridge Interface

Referring again to the DMM/switch example described above, a VXI switch and an LXI DMM can handshake using either LAN-based messaging or hardware triggers through the slot 0 bridge. From a hardware perspective, the eight-line LXI M-LVDS trigger bus and the eight-line VXI TTL trigger bus are unified without the need for external-level translators.

SUMMARY

In just four years, LXI has proven to be a capable communications platform and successor to GPIB, with additional benefits resulting from its Ethernet core. Demanding test and data acquisition applications, however, present challenges in synchronization and module-to-module communication that are difficult to overcome with discrete standalone instruments designed to the minimum LXI Class C specification. In contrast, modules in mainframe-based systems share resources by plugging into a common backplane, which makes them inherently synchronized and highly deterministic. To best emulate the performance of a mainframe platform, next generation LXI Class A instruments uniquely provide a distributed backplane for standalone instruments and the optimal combination of low cost and high performance that can address a broad range of applications.

About the Author

Tom Sarfi joined VTI in 1997 as applications engineering manager and currently is their business development manager for functional test. Prior to joining VTI, he was a development engineer on the ATE systems team for Westinghouse Naval Systems Division. Mr. Sarfi earned a B.S.E.E degree from Case Western Reserve University, Cleveland, OH.

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